chip, which may be programmed to be inserted on any specific scanline of the video output. The primary purpose of this pin is to automatically alert the processor **102** at a fixed time, prior to the starting of the next displayed frame. By receiving an interrupt with known timing that is relative to the display operation, the processor **102** can reconfigure the current display state for primary display controller **104**—controlled refresh, or secondary display controller **106** controlled refresh, without "busy-wait" or polling loops. See DCONLOAD below for further details.

[**0063**] DCONBLNK is used to provide assistance on occasions when it is desirable to asynchronously initiate a display change in the display state. The secondary display controller **106**, which is intended to be polled, will drive the DCONBLNK output under two circumstances. Under the first circumstance, the DCONBLNK output is driven low at the beginning of the first output scan line, following the active Vertical Resolution output scan lines, and remains low until the trailing edge (end) of the output Vsync timing interval, at which point it is driven high again. In the second circumstance, the DCONBLNK output remains high whenever the display of the output of secondary display controller **106** is disabled.

[**0064**] DCONSTAT is used to indicate whether primary display controller **104** or secondary display controller **106** is currently managing managing the display refresh. Since the display control switching of secondary display controller **106** is synchronous with the display process, the status pin allows the processor **102** to identify precisely when the display switching of secondary display controller **106** occurs.

[**0065**] DCONLOAD is used to initiate a Display Load frame-loading cycle. This signal indirectly determines whether the video timing outputs of secondary display controller **106** follow the video inputs or whether the internal timing registers of secondary display controller **106** are driving the video outputs. Please note that in either case the actual data outputs made to the panel will normally be modified by the secondary display controller **106** chip, as discussed in secondary display controller **106** Display Mode register description, above.

[**0066**] Secondary display controller **106** Display Controller ASIC Pinout—2M (1M×16)

[**0067**] DRAM Configuration

[**0068**] Geode Display Interface Pins

[**0069**] Geode Pixel Clock GFDOTCLK 1

[**0070**] Geode Red Data GFRDAT0-4 5

[**0071**] Geode Green Data GFGDAT0-5 6

[**0072**] Geode Blue Data GFBDAT0-4 5

[**0073**] Geode Vsync GFVSYNC 1

[**0074**] Geode Hsync GFHSYNC 1

[**0075**] Geode Display Enable GFDISP_EN 1

[**0076**] Geode FP_LDE GFP_LDE 1

[**0077**] Interface Pins for 1M×16 DRAM

[**0078**] FBRAM Data FBD0-15 16

[**0079**] FBRAM Address FBA0-11 12

[**0080**] FB Column Addr Strobe FBCAS/1

[**0081**] FB Row Addr Strobe FBRAS/1

[**0082**] FBRAM Chip Select FBCS/1

[**0083**] FBRAM Write Enable FBWE/1

[**0084**] FBRAM Clock FBCLK 1

[**0085**] FBRAM Clock Enable FBCLKE 1

[**0086**] Crystal for secondary display controller **106** Self-Refresh

[**0087**] Display XTAL In DCONXI 1

[**0088**] Display XTAL Out DCONXO 1

[**0089**] System Interface Pins

[**0090**] System Reset RESET 1

[**0091**] secondary display controller **106** Interrupt Output DCONIRQ/1

[**0092**] secondary display controller **106** Display Load Command Request DCONLOAD 1

[**0093**] secondary display controller **106** vs. Geode/Display Active Status DCONSTAT 1

[**0094**] secondary display controller **106** Blanking Status DCONBLNK 1

[**0095**] secondary display controller **106** Register I/O SMB Clock DCONSMBCLK 1

[**0096**] secondary display controller **106** Register I/O SMB Data DCONSMBDATA 1

[**0097**] PPTTL/Panel Interface Pins

[**0098**] Panel Pixel Data 1 D1O0-2 3

[**0099**] Panel Pixel Data 2 D2O0-2 3

[**0100**] SCLK SCLK 1

[**0101**] DCLK DCLK 1

[**0102**] GOE GOE 1

[**0103**] GCK GCK 1

[**0104**] GSP GSP 1

[**0105**] DINT DINT 1

[**0106**] SDRESET SDRESET 1

[**0107**] DBC DBC 1

[**0108**] INV INV 1

[**0109**] PWST PWST 1

[**0110**] POL1 POL1 1

[**0111**] POL2 POL2 1

[**0112**] Self-Test/Boundary Scan BIST0-1 2

[**0113**] Total User I/Os 84

REGISTER DEFINATIONS

Register **0**: Secondary Display Controller **106** ID+Revision

[**0114**] This 16-bit register is a read/only-register that returns secondary display controller **106** ASIC identifier and the revision number. The first pass of this silicon should